IN THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

1. (Original) A data processing apparatus comprising:

a plurality of first cells having n-bit (n: natural number) input/output ports and performing ALU processing; and

one or a plurality of second cells having n-bit input/output ports and performing bit processing,

wherein the cells are connected through a network with n-bit buses.

2. (Original) The data processing apparatus according to claim 1, wherein said second cell fixes bits of orders irrelevant to outputs to "0" or "1" when the number of output bits is smaller than n.

3. (Original) The data processing apparatus according to claim 2, wherein said second cell comprises:

a circuit that realizes an arbitrary logic function with n-bit inputs and 1-bit output; and

a circuit that divides the output into n bits and masks the divided n-bit signals arbitrarily.

4. (Original) The data processing apparatus according to claim 1, wherein a carry-out of ALU in one first cell and a carry-in of ALU in another first cell are connected.

5. (Currently Amended) The data processing apparatus according to claim 4, wherein:

a logic circuit of the second cell is used as a circuit that realizes an arbitrary logic function with (n+1)-bit inputs and 1-bit output;

a carry-out of ALU in one first cell is used as an input to said second cell; and

the output of the logic circuit of said second cell is connected to a carry-in in another <u>first</u> cell [~~A~~].